STUDIES ON Si-SiO_2 INTERFACE OF THERMALLY OXIDIZED SILICON SURFACES

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CERTIFICATE

This is to certify that the thesis entitled "Studies on Silicon-Silicon Dioxide Interface of Thermally Oxidized Silicon Surfaces" by Iqbal Singh is a record of work carried out under my supervision and has not been submitted elsewhere for a degree.

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A B S T R A C T

The work reported in this thesis aims at setting up adequate facilities for thermal oxidation of silicon for growing high quality silicon dioxide films. Procedures, precautions and other useful aids which were found necessary for producing good quality oxides have been described in detail. An MOS structure was fabricated and used to measure the important properties such as dielectric constant and breakdown field strength of the grown oxide films.

The $Si-SiO_2$ interface has been investigated both at high as well as at low frequencies using the same MOS capacitor as a function of applied bias. The density of surface states on this interface has been found to be 4.6×10^{11} states/cm^2 which is in fairly good agreement with the values obtained by other workers. Other results obtained during these investigations are also in close agreement with those cited in the literature as can be seen from the concluding remarks.

LIST OF SYMBOLS

d_{ox} – oxide thickness

t – time for oxidation

c – rate constant

T – constant

ϕ – potential difference between the bulk and space charge region

ϕ_s – surface potential

ϕ_B – bulk potential

ϵ_{ox} – oxide permitivity

ϵ_s – semiconductor permitivity

ρ – charge density

L_D – Debye length

k – Boltz mann constant

T^o – absolute temperature

q – electronic charge

n_i – intrinsic carrier concentration

N_A – acceptor doping concentration

u – $\frac{q\phi}{kT}$

u_s – $\frac{q\phi_s}{kT}$

Q_{sc} – space charge density

Q_{ss} – surface state charge density

C_{sc} – surface space-charge capacitance

C_{ss} – surface state capacitance

X_d – thickness of space-charge region

V_{app} - applied voltage

C_{meas} - measured capacitance

Q_p - charge on the gate

V_{ox} - voltage drop across the oxide

ϕ_{so} - ϕ_s with vapp =0

C_n - $\frac{C}{C_{ox}}$ normalised capacitance

Y - Surface potential relative to the bulk

β - $\frac{q}{kT}$

V_{FB} - flat band voltage

ϕ_{ms} - metal-semiconductor work function difference

χ - electron effinity

N_{ss} - density of surface states

ABBREVIATIONS

MOS - Metal-oxide-semiconductor

TCE - Trichloroethylene

C O N T E N T S

Chapter I

INTRODUCTION

Roles of Oxides in Electron Device Fabrication

Silicon-based discrete devices and specially integrated circuits play an essential and ever increasing role in the electronics industry now-a-days. Silicon oxides are extensively used in the fabrication of these devices and ICs, to serve one or more of the following purposes:

(a) Masking for selective diffusion of impurities.

(b) Primary surface passivation and stabilization.

(c) Dielectric isolation, and

(d) Active device dielectric.

A brief description of all these roles is given below:

Oxide masking:[1,2,3] Oxide masks are invariably employed for selective diffusion of certain impurities, particularly phosphorus and boron in silicon for planar diffused junction formation. The mechanism of the masking action of an oxide involves its conversion into a mixed oxide of SiO_2 with P_2O_5 or B_2O_3. Both P_2O_5 and B_2O_3 diffuse into the oxide, replace the silicon atoms with phosphorus or boron atoms and convert the oxide into a different type of glass. The boundary between the phosphorus or boron-containing top layer and the remaining part of the oxide

film has been found to be very sharp and well defined. Diffusion of P_2O_5 or B_2O_3 in advance of this boundary is negligible, SiO_2 films are thus most effectively used for selective masking of impurities in the planar technology.

Surface Passivation[4]: Stability and reproducibility of the silicon device characteristics are greatly improved by passivating the sensitive device surfaces. Ordinarily, passivation is defined as a process of rendering a surface nonreactive by forming a layer which inhibits further reaction. In the case of semiconductors, chemical as well as electrical stability are required in a passivated surface. Hence the passivation of a semiconductor surface is completed in two stages. Firstly, there is the primary passivation for control and stabilization of the electrical properties of semiconductor surface. The primary passivation uses a grown SiO_2 layer on the semiconductor surface to be passivated. The oxide layer in turn is protected and stabilized by the secondary passivation layer which is obtained by deposition of another passivation material such as phosphosilicate glass, silicon nitride etc. which are very inert materials hence are suitable for chemical passivation. The second passivation layer also performs the function of insulating and protecting the interconnection and terminal metallurgy, and providing overall mechanical and chemical protection.

Dielectric Isolation for Electrical Insulation:

Carefully grown oxide films possess good insulating properties such as low pin hole density, high breakdown strength, high dielectric sonstant and low dielectric losses. Such high quality oxide films are most frequently used for dielectric isolation in ICs, these days.

The convenience and ready availability of silicon oxide also make it a natural choice for the dielectric of the MOS capacitors, often used in IC functional blocks. The dissipation factor, breakdown voltage and temperature coefficient of capacitance of silicon oxide are also suitable for this application.

Active Device Dielectric: In MOS devices, the dielectric film used as the gate insulator is an active integral part of the device so that the device characteristics are very sensitive to its properties. Hence in MOS technology, emphasis is placed on the fabrication of this oxide rather than on diffusion. To achieve this end cleanliness must be maintained throughout the complete procedures of oxide formation. The problems which one faces in producing high quality oxide film are described in Chapter IV of this report.

Some devices in which oxide dielectric film is an active functional part of the device are MOS transistor, surface tetrode and various other three or four junction

devices. Since the characteristics of these devices are sensitive to fluctuations in interface properties, their fabrication depends more strongly upon surface control and stability. For such applications only very superior quality oxides can be employed which is not too difficult to achieve with the sophisticated oxide formation techniques at the present state of silicon technology.

By this time, enough has been said about the vital role of the oxides in the fabrication of silicon planar devices and integrated circuits.

The primary objective of the present work was to set up necessary facilities for thermal oxidation of silicon, so that no difficulties are encountered at a later stage and oxidation becomes a routine process when work on planar technology and IC fabrication is started. Special efforts have gone to obtain good quality oxide of reproducible properties suitable for the above applications.

To ensure that the grown oxide be of good quality following criteria were thought to be necessary. The grown oxide film must have:

(a) Good insulating properties which implies
    (i) Low pin hole density
    (ii) High dielectric strength
    (iii) High resistivity
    (iv) Dielectric constant that is close to the reported value for silica glass,
    (v) Low dielectric losses.

(b) Low and reproducible density of surface states.

(c) Resistance to ambient stress especially no or minimum ionic motion at elevated temperature and/or high field.

To measure these properties an MOS structure was thought to be suitable and has been used throughout these investigations.

The work presented in this report is partly theoretical and partly experimental. Chapter II of this work deals with the methods of oxide formation and various mechanisms involved in oxide growth. Chapter III is devoted to theory of semiconductor surfaces and important properties of the silicon-silicon dioxide interface. This knowledge is essential for the understanding and interpretation of the various curves obtained from the measurements in Chapter V. Chapter IV forms the heart of this report and deals with the complete fabrication techniques of MOS structure. Cleaning operations that were found necessary to obtain good quality oxide film have been described in detail and a routine procedure has been established for obtaining sufficiently good oxide layer that could be used in the fabrication of passive components, planar diffused transistors and integrated circuits. In Chapter V various measurement techniques and results of measurements have been reported. In concluding remarks, a comparison is made between the values of various quantities such as dielectric strength, density of surface states etc. as reported in the literature and obtained in the present work.

Chapter II

METHODS OF OXIDE FORMATION AND OXIDE GROWTH MECHANISM

According to the methods of preparation, silicon oxides can be broadly classified as

(a) Thermal oxides

(b) Anodic oxides

(c) Deposited oxides.

Thermal Oxides: "Thermal Oxides" are those oxides which are formed from a thermally activated reaction of silicon with oxygen, water, or other oxygen bearing species. Thermally grown oxides are most widely used as a mask against impurity diffusion and passivation layer at the semiconductor surface.

In the present work only thermal oxidation of silicon was employed so that this method is described in detail. Other methods are mentioned only for the sake of completeness.

Oxides can be grown thermally on silicon surface by any one of the following four processes:

(a) Steam oxidation

(b) Oxidation in dry oxygen

(c) Wet oxygen oxidation, and

(d) Accelerated oxidation.

2.1 Steam Oxidation of Silicon[5]

The reaction of high temperature water vapor with silicon is called steam oxidation only when the quantity of vapor present does not limit the oxidation rate. The growth of few initial layers of oxide prevents further contact between the reactants. Several monolayers of oxide are formed by chemisorption of water. Further growth requires the transport of one of the reactants through the already existing oxide.

Reaction kinetics: After the first few layers of oxide are formed, preventing further direct contact of water with silicon, the reaction is supposed to proceed between either interstitial water molecules in the oxide and silicon atoms bound to the silicon lattice[5],

$$H_2O + Si\text{-}Si \rightarrow Si\text{-}O\text{-}Si + H_2 \qquad (2.1)$$

or from the reaction of an intermediate silicon hydrooxide group (silanol group) and silicon. In the latter mechanism the following reactions occur in the neighbourhood of the gas-oxide interface:

$$\underset{\text{vapor}}{H_2O} + \underset{\text{oxide}}{S_i - O - S_i} \rightarrow \underset{\text{silanol}}{2(Si - OH)} \qquad (2.2)$$

and at the oxide-silicon interface, the reaction is

$$2(Si\text{-}OH) + Si - Si \rightarrow 2(Si\text{-}O\text{-}Si) + H_2 \qquad (2.3)$$

In the above reaction H_2 produced during the oxide formation diffuses rapidly away from the oxide-silicon interface.

In both oxide forming reactions, described in eqn.(2.1) and eqn.(2.3), the species combining with the silicon must diffuse through the existing oxide layer to reach the oxide-silicon interface.

At usual oxidation temperatures the diffusion coefficient of hydrogen in bulk silica is several order of magnitude larger than that of steam[2] so that hydrogen diffuses much faster than water and permits the oxidation to be limited, presumably by the availability of molecular water and/or hydroxyl groups at the interface.

For steam oxidation above 1100°C the oxide growth is limited by diffusion of the oxidising species through the film, the growth is parabolic given by[5]

$$d_{ox}^2 = c\ t \qquad (2.4)$$

where d_{ox} is oxide thickness,

t is time for oxidation, and

c is rate constant.

Below 1100°C the relationship found experimentaly by Deal and Grove[4] is given by[6]

$$d_{ox}^2 + A\ d_{ox} = B(t + T) \qquad (2.5)$$

The constants A and T are only of importance for thin oxide films. The linear growth probably occurs when the chemical reaction rate at the oxide-silicon interface rather than the supply of the reactants limits the oxidation (eqn.2.1).

Additional evidence for the reaction rate limitation exists in the observed dependence of oxide growth upon orientation[7]. In the linear growth regions, the reaction rate depends upon the number of silicon bonds that are available to react with the water molecule at the oxide-silicon interface. This dependence of oxidation rate upon orientation has been confirmed experimentally in high pressure steam oxidation; the oxidation rate are in the order (110) orientation > (311) orientation > (111) orientation.

In steam oxidation of silicon at atmospheric pressure, only the low temperature, nonparabolic oxidations show a dependence on orientation. If the previously described kinetic picture is correct, the high temperature parabolic oxidations should not be influenced by factors that affect only the interface reaction rate (such as silicon substrate orientation), since this factor is not the primary rate limiting factor in that temperature range. The temperature at which orientation dependences appear can be regarded as those at which the interface reaction is beginning to limit the growth rate of oxide.

2.2 Oxidation of Silicon in High Pressure Steam

It has been found that oxide films of good quality can be grown by oxidation at relatively low temperatures if the water pressure is increased to several atmospheres[7]. Within a certain range of pressures and temperatures uniform films could be made, the growth rate of which

appeared to be linear in time and directly proportional to the steam pressure. At excessively high pressures, however, the oxide film may dissolve in the steam phase, so that no growth occurs. The time-independent growth rate indicates that the rate determining step in this oxidation method is the oxidation of the silicon at the $Si-SiO_2$ interface.

2.3 Oxidation of Silicon in Dry Oxygen

This is the method of oxidation that has been employed in present work for preparing the MOS structure for surface state and barrier height measurements. In dry oxygen oxidation the species diffusing through the growing oxide layer is supposed to be oxygen ions[8]. The growth of oxide by this method can be influenced by the application of an electric field . Conventional marker and radio-active tracer experiments have shown that the oxide grows at the oxide-silicon interface rather than the oxide-gas interface.

Reaction kinetics in dry oxidation: As in steam oxidation lower temperature oxidation kinetics seen to be limited by the reaction at the interface rather than the diffusion of oxygen ions. The growth departs from parabolic and becomes more linear at temperature under 1000°C.

The high activation energy of dry oxygen oxidation reflects the tight bonding of oxygen ions in the oxide.

2.4 Wet Oxygen Oxidation of Silicon

For this project, this method of oxide formation was employed for making MOS structure for dielectric strength and dielectric constant measurements of the oxide film. In wet oxidation the dry oxygen is passed through a water bath containing very pure distilled DI water, having the resistivity of the order of 15 Mega-ohms cm., prior to being introduced into the oxidation furnace. The oxidation rate can be increased by increasing the water-vapour pressure, i.e., by increasing the temperature of the water bath. In this process of oxidation concentration of the oxidizing species can be easily varied, which is not possible either in the dry oxygen system or the steam oxidation system. In the wet oxygen system, however, the oxidizing species is a mixture of oxygen and "water" whose ratio is determined by the mixing of water vapour with oxygen. In principle it is possible to vary the oxidation rate from that of 100% oxygen to that of nearly 100% water vapour. In this work, water bath temperature was kept at 90°C and flow of oxygen gas was maintained at 1 litre/minute. The dry oxygen used as carrier gas was filtered by passing through a micron filter before bubbling through the water bath. The water used was of high purity. Water bath also acts as a filter and seems to remove many of the particles that a submicron filter catches. The temperature for oxidation was 1150°C.

2.5 Description of the Oxidation Set-up used in the Present Work

Oxides were grown at atmospheric pressure by open tube oxidation method. A 60 mm. dia. and 60" long high quality quartz tube with its one end open to atmosphere has been used. The quartz tube is heated in a furnace "Thermco Spartan" supplied by Thermco Products Co. Orange Calif., U.S.A. This furnace employs resistance heating for heating the work tube. Temperature of the furnace remains stable within $\pm\frac{1}{4}$°C in a flat zone length of 24" in the centre of the tube

Oxygen is made to pass through a micron filter and a dryer (moisture trap) before entering the work tube in case of dry oxidation, while in case of wet oxidation, it is bubbled through a bubbler containing very pure water at desired temperature. The oxidation system which has been supplied by Fischer and Porter Company, Berkeley Glass Lab. Division, U.S.A. has a flask of pyrex glass of one litre capacity fitted with a thermometer pocket for measuring the temperature of water bath. A pressure release valve which operates when the pressure inside the flask exceeds the preset value, is also provided for safety purposes. In addition to this, the system also consists of one 3-way and one 2-way solenoid valves which make the system capable of doing steam, wet and dry oxidation. The normally closed end (NC) of the 3-way value is connected to the bubbler (Figure 1). The 2-way valve which is connected at the output

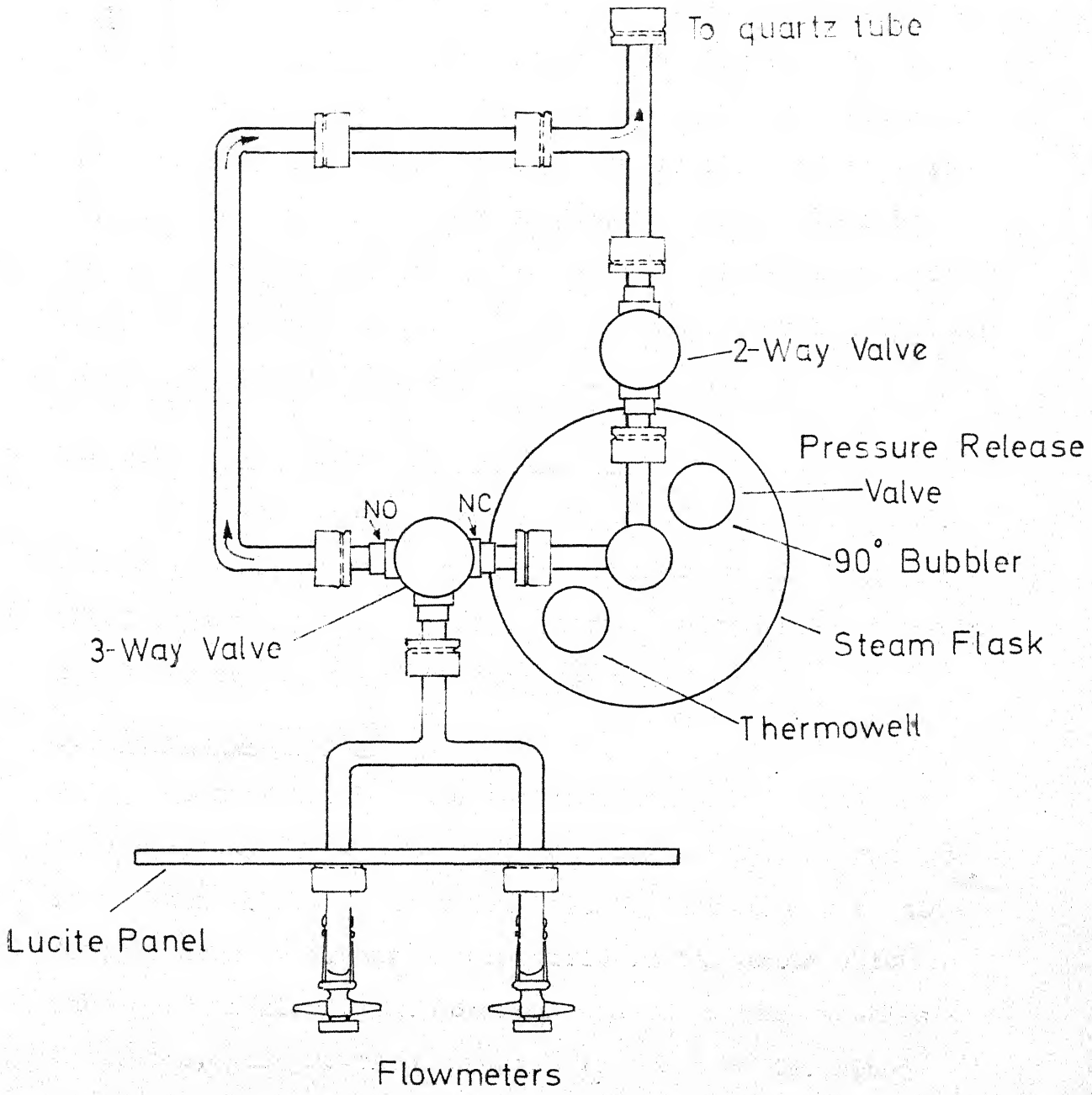


FIG. 1 OXIDATION SYSTEM

This system is capable of doing steam wet and dry oxidation

is normally closed. Hence, until the valves are energized by switching on to the power supply, oxygen is not permitted to enter the bubbler and it takes an alternative path provided for this purpose as marked in the Figure 1 by thick arrows. As soon as the values are energized by operating the power supply switch, oxygen flow is directed to pass through the bubbler and wet oxidation starts. Thus by merely operating a power supply switch, we can switch from dry to wet or wet to dry oxidation. Thus many combination of oxidation process can be used if desired.

2.6 Accelerated Oxidation of Silicon

The temperature necessary for oxide-film formation can be lowered by rate-accelerating additives. Lead oxide (PbO) especially has appeared to be a suitable accelerating agent and may be added through the vapour phase.

2.7 Anodic Oxidation[9]

Silicon can be oxidized anodically in a suitable electrolyte. The growth of anodic oxide films on silicon in a liquid electrolyte which does not dessolve the oxide depends upon an electrostatic field in the oxide which enhances ion migration. Si ions are the mobile species; therefore, the growth of anodic oxide can be described by the transport of Si ions across the oxide-silicon interface through the oxide to the oxide-electrolyte interface where an oxidation reaction takes place.

Since oxide films obtained by anodic oxidation have a much larger content of ionic impurities than films made by thermal oxidation, so they have not yet found many applications in semiconductor device technology.

2.8 Deposited Oxides[10]

Deposited oxides include all those oxides formed by methods not requiring the silicon substrate to participate in the oxide forming reaction. Hence a substrate can be a material other than silicon, so that the results may be applicable to Ge, GaAs etc. Three techniques commonly employed to deposite oxide films are pyrolysis, vacuum evaporation and reactive sputtering.

Chapter III

SEMICONDUCTOR SURFACES AND SILICON-SILICON DIOXIDE INTERFACE

Surfaces play an important role in the operation of semiconductor devices. Apart from those devices whose operations depend solely on surface properties such as MOS transistors, they also influence the behaviour of devices involving p-n junctions.[11,12]

3.1 Methods of Surface Investigations

Commonly employed methods for semiconductor surface investigations include:

(1) Field effect experiment, and

(2) MOS structure.

In field effect experiment, the surface conductance is varied by the application of an electric field normal to the surface. To draw conclusions about the behaviour of surfaces from the field effect experiments a knowledge of carrier mobility at the surface is essential. Because of the various surface scattering mechanisms the mobility at the surface may be quite different from that in the bulk and it is generally difficult to estimate its value. The MOS technique does not require any knowledge of surface mobility. In this method, instead of conductance, the capacitance of

semiconductor surface is studied as a function of the electric field normal to the surface. This technique has been employed for studying the behaviour of silicon-silicon dioxide interface since an MOS structure which includes this interface provides a convenient capacitor. Essentially, this technique of surface investigations depends on the interpretation of the deviations between an idealised theory and experimental observations. In the work described in this report, this technique has been invariably used in all the investigations. This chapter provides the theoretical background necessary for the interpretation of experimental results described in Chapter V.

3.2 Surface Space-Charge Region[13,14,15]

The region near the surface of a semiconductor associated with the surplus (accumulation) or deficit (depletion) of free charge carriers as compared to that of the bulk is called surface space charge region. This region can be produced either by an electric field outside the semiconductor or by contacting the semiconductor with a metal or insulator with different work function. Surface space-charge region can also be produced by "surface states" located on or near the semiconductor surface.

Appearance of space-charge results in the band bending near the surface which in turn gives rise to a

potential difference (ϕ) between the bulk and the space-charge region. Value of this potential difference at the surface ϕ_s is known as "surface potential". The value of ϕ in the bulk given by $q\phi_B = E_F - E_i$, is called the bulk potential.

The potential and field distribution in the space-charge region is obtained by solving the Poission's equation,

$$\frac{d^2\phi}{dx^2} = -\frac{\rho}{\epsilon_s} \qquad (3.1)$$

where ρ is the charge density and ϵ_s is the permittivity of the semiconductor material.

For a non-degenerate semiconductor, equation (3.1) can be written in the form[14]

$$\frac{d^2u}{dx^2} = \frac{1}{L_D^2}(\text{Sinh } u - \text{Sinh } u_B) \qquad (3.2)$$

where

$$u = \frac{q\phi}{kT} \quad \text{and} \quad L_D = \left(\frac{\epsilon_s kT}{2q^2 n_i}\right)^{\frac{1}{2}} \qquad (3.3)$$

is known as Debye length.

Solution of equation (3.2) after some simplification yields,

$$Q_{sc} = 2qn_i L_D F(u_S - u_B) \qquad (3.4)$$

where Q_{sc} represents the charge in the surface space-charge

region, and $F(u_S, u_B)$ has been substituted for

$$\sqrt{2}\left[\text{Sinh } u_B(u_B-u_S)-(\text{Cosh } u_B-\text{Cosh } u_S)\right]^{\frac{1}{2}}$$

Where $u = u_B$ when $\phi = \phi_B$ and $u = u_S$, when $\phi = \phi_s$.

3.3 The Ideal MOS Structure[16]

In an ideal MOS structure, the surface states and presence of charge in the oxide layer are absent. Also, the effect of work function difference between the metal and semiconductor is neglected. The applied voltage, therefore, will partly appear across the oxide and partly across the silicon. Thus

$$V_{app} = V_{ox} + \phi_s \tag{3.5}$$

where V_{app} is the applied voltage, and V_{ox} is the voltage drop across the oxide layer.

Since there are no charge traps, the whole charge appears in the space-charge region, so equation (3.5) can be written as

$$V_{app} = -\frac{Q_{sc}}{C_{ox}} + \phi_s \tag{3.6}$$

The small signal capacitance of such a MOS structure can be considered as the capacitance due to the oxide film C_{ox} in series with the space charge capacitance C_{sc}, so that the total capacitance is given by

$$C = \frac{C_{ox}\, C_{sc}}{C_{ox}+C_{sc}} \tag{3.7}$$

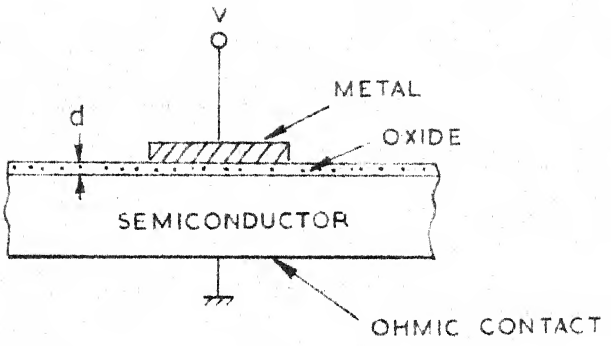


FIG. 2a METAL-OXIDE-SEMICONDUCTOR (MOS) STRUCTURE

In equation (3.7) C_{ox} is constant, but C_{sc} depends on the thickness of the space-charge region and is given by

$$C_{sc} = -\frac{dQ_{sc}}{d\phi_s} = \frac{\epsilon_s}{x_d} \quad \text{per unit area} \qquad (3.8)$$

Here x_d is the thickness of space-charge region. Elimination of x_d between equations (3.7) and (3.8) yields the relation for a p-type semiconductor

$$\frac{C}{C_{ox}} = \frac{1}{1+\left(\frac{2\epsilon_{ox}^2}{qN_A\epsilon_s d_{ox}^2} V_{app}\right)^{\frac{1}{2}}} \qquad (3.9)$$

which predicts that the capacitance will fall with the square root of the applied voltage while the surface is being depleted.

Typical shapes of theoretical C-V curves for MOS structures on p-type and n-type material are given in Figures 2 and 3 respectively.[17] Qualitatively the shape of these curves can be explained as follows:

Considering p-type material, a negative charge on the metal electrode (gate) will cause accumulation of holes at the surface. Variations in charge by the a.c. measuring signal then occurs so close to the $Si-SiO_2$ interface that C_{sc} in equation (3.7) is large compared to C_{ox}. The measured capacitance thus approaches C_{ox} for a negative voltage on the gate. When the negative bias is low, i.e., when the band bending at the silicon surface is slight, the space-charge variations due to the measuring

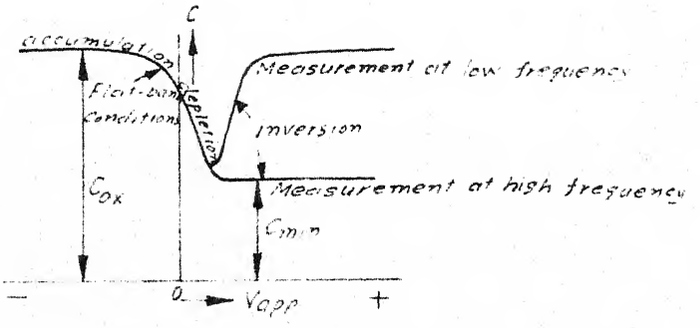


Fig. 2 Theoretical C-V curve of an MOS structure on p-type silicon for high and low frequencies

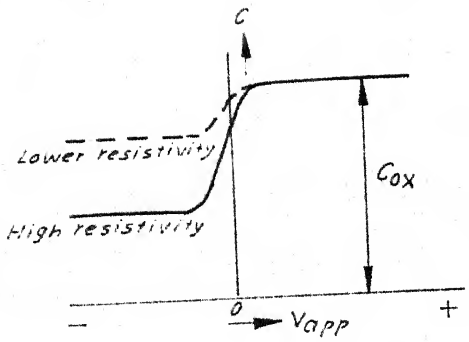


Fig. 3 High frequency theoretical C-V curve of anMOS structure on n-type silicon

signal no longer occur very close to the interface. Consequently C_{sc} becomes comparable to C_{ox}. This results in lowering the value of overall capacitance of the MOS structure at zero or very small electrode voltage. The measured small signal capacitance of an MOS structure, in the absence of any d.c. bias applied to gate, is referred to as "Flat Band Capacitance". The value of flat band capacitance is less than the capacitance of oxide layer alone.

When the d.c. bias at the gate is increased from zero to positive values a depletion layer forms at the silicon surface. An increase in the negative charge in this layer is accompanied by an increase in the depletion region thickness. The a.c. signal causes charge variations at the edge of the space charge region. When the d.c.bias is increased it looks as if the distance between the two electrodes of MOS capacitor becomes larger, so that the capacitance decreases. However, at a sufficiently high voltage the band bending becomes so large that a layer of free electrons can be formed at the surface. As this inversion layer is very close to the Si-SiO_2 interface, the effective capacitance at low frequencies (below 100 Hz/sec.) may again become equal to C_{ox}, the oxide capacitance alone as shown by the dotted curve in Figure 2.

3.4 Frequency Effects[16,17]

Capacitance increase in the inversion region occurs only when the measuring frequency is sufficiently low usually less than 100 Hz/sec. At such low frequencies the recombination-generation rates of electron-hole pairs in the depletion region can keep up with the measuring signal variations so that the charge exchange with the inversion layer is possible. At higher frequencies, however, the supply of charge carriers to the inversion layer is difficult because these (minority) carriers cannot be generated quickly enough. As a result, the effective capacitance decreases and reduces to a value C_{min} shown in Figures 2 and 3.

The minimum capacitance is closer to C_{ox} in the case of lower resistivity silicon. Low resistivity silicon approaches the nature of metal and hardly any change in capacitance occurs when the gate voltage is varied from zero to sufficiently high values. This has been observed in the present work when an attempt was made to measure the surface state density of the Si-SiO_2 interface using an MOS structure constructed from a 0.4 ohm cm. silicon crystal ($1x10^{16}$ donors/cm^3) at the earlier stages of this work. No noticeable change could be obtained in capacitance inspite of sufficiently large voltage applied at the gate.

3.5 Practical MOS Structure[16-24]

A practical MOS structure differs from an ideal one described above, in the following respects:

(a) presence of surface-states on the $Si-SiO_2$ interface,

(b) presence of fixed charge at the oxide surface,

(c) presence of the mobile ions within and on the surface of the oxide layer,

(d) presence of the difference in the metal-semiconductor work function.

Effects of these deviations on the properties of a practical $Si-SiO_2$ interface will now be considered in some detail.

(a) Surface States[18] Surface states have traditionally been classfied as (i) Fast surface states, and (ii) Slow surface states depending upon their time constant.

Fast Surface States: The termination of the periodic crystal lattice at the surface gives rise to unsaturated or "dangling bonds". The surface atoms having these unsaturated bonds act as acceptor states in the sense that they can trap electrons. These states correspond to energy levels in the forbidden energy gap of the semiconductor. On a "clean surface" the number of such states has been observed to be of the order of 10^{14} to 10^{15} states/cm^2 which agrees with the theory. On real surfaces, the density and distribution of surface states are altered by

adsorbed molecules and ions and oxide growth defects. The formation of oxide layer and absorbed impurities present on the surface use up most of the unsaturated or "dangling bonds" through new bond formation, thus reducing the density of fast surface states to the order of 10^{11} to $10^{12}/cm^2$. Depending upon the crystal structure and surface treatment, the silicon surface may assume an acceptor like or donor like nature.

According to Revesz[25], fast surface states can also appear at the interface due to the formation of trivalent silicon under certain conditions of oxide growth. This trivalent silicon behaves as donor state in the following fashion

$$S_i^{3+} = S_i^{4+} + \bar{e}$$

Effects of Surface state on the properties of silicon-silicon-dioxide interface:

The electrons trapped in the surface states induce a sheet of negative charge (Q_{ss}) on the interface of the $Si-SiO_2$ system. This charge on the surface induces an equal amount of charge of opposite polarity in side the semiconductor and hence leads to the appearance of a space-charge region near the semiconductor surface. A differential capacitance (C_{ss}) will be associated with the surface state charge (Q_{ss})

$$C_{ss} = \frac{dQ_{ss}}{d\phi_s} \qquad (3.10)$$

MOS Structure in the Presence of Fast Surface States:

A quantitative description of the effects of surface states on the behaviour of the $Si-SiO_2$ interface will now be presented.

The capacitance of the device is given by the expression

$$C_{meas} = \frac{dQ_p}{dV_{app}} \qquad (3.11)$$

where Q_p is the charge on the gate electrode and V_{app} is the applied voltage.

Since the net charge in the system is zero, we must have

$$Q_p + Q_{ss} + Q_{sc} = 0 \qquad (3.12)$$

The applied voltage neglecting the difference in contact potential, can be written as

$$V_{app} = V_{ox} + (\phi_s - \phi_{so})$$

where ϕ_{so} is the value of ϕ_s in the absence of applied voltage.

If there is no charge in the oxide layer, then

$$V_{app} = -\frac{(Q_{ss} + Q_{sc})}{C_{ox}} + (\phi_s - \phi_{so}) \qquad (3.13)$$

From equation (3.13) we obtain

$$\frac{dV_{app}}{d\phi_s} = C = 1 + \frac{C_{ss} + C_{sc}}{C_{ox}} \qquad (3.14)$$

as the capacitance of the device.

Also from equation (3.12), we get

$$\frac{dQ_p}{d\phi_s} = C_{ss} + C_{sc} \tag{3.15}$$

Therefore, from equation (3.11), we get

$$C_{meas} = \frac{dQ_p/d\phi_s}{dV_{app}/d\phi_s} \tag{3.16}$$

or

$$C_{meas} = \frac{C_{ss} + C_{sc}}{1 + \frac{C_{ss}+C_{sc}}{C_{ox}}} \tag{3.17}$$

From equations(3.14) and (3.15),

$$\text{or} \quad C_n = \frac{C_{meas}}{C_{ox}} = \frac{C_{ss} + C_{sc}}{C_{sc} + C_{ss} + C_{ox}} \tag{3.18}$$

The form of equation (3.18) indicates that the oxide capacitance C_{ox} is in series with the parallel combination of the surface state capacitance and the space charge capacitance as shown in the equivalent circuit of Figure 4

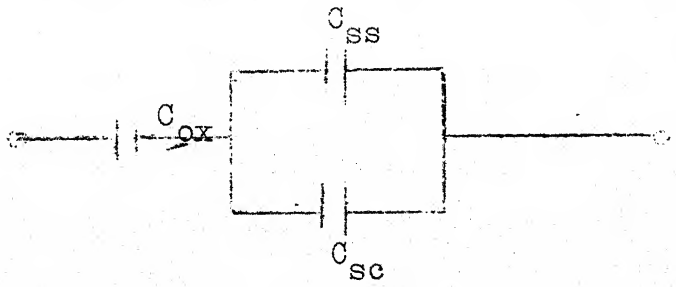


Fig.4

Equivalent circuit of MOS structure in the presence of surface states.

(b) Oxide Charge:[16,18,24] (Surface and Space Charge).

Oxide charge includes the charge on the surface as well as in the bulk of the oxide layer. The surface charge is composed of the fixed charges, the mobile ions and the ionized traps which are located near or at the $Si-SiO_2$ interface. The fixed surface charge has the following properties: it is fixed and is not influenced by applied voltage over a wide variation of surface potential (ϕ_s). It is located within the order of 200 Å of the $Si-SiO_2$ interface,[18] its density (Q_{fc}) is not greatly affected by the oxide thickness or by the type or impurity concentration in the semiconductor. Q_{fc} depends on the oxidation growth, annealing conditions and on the semiconductor orientation. It has been suggested[18] that the excess ionic silicon in the oxide is the origin of the fixed surface charge in the $Si-SiO_2$ system. The effect of the fixed charge on the MOS capacitance curve is a parallel shift of the curve along the voltage axis, and the amount of shift is given by

$$V = \frac{Q_{fc}}{C_{ox}}$$

(c) Mobile Ions in the Oxide Layer:[16,18]

Presence of the mobile ions (especially N_a^+ ions) in the bulk of MOS devices renders the device characteristics unstable. The flat band voltage is subjected to drift under bias at elevated temperatures. This drift is caused by the

rearrangement of the ionic space charge distribution within the oxide. The mobile M_a^+ impurity, being due to an external contamination could be eliminated or atleast minimised by appropriate precautions in the device fabrication procedure. Once this contamination is eliminated MOS device becomes stable even under bias at elevated temperatures.

(d) Effect of Metal-Semiconductor work Function difference on MOS Characteristics:[16]

When a semiconductor material is in the intimate contact of a metal with different work function, the electrons will flow from the metal into the semiconductor or vice-versa until thermal equilibrium is reached and a voltage equal to this work function difference appears between the two. This tends to widen the space charge region already existing due to surface states and the oxide charge. Thus effect of the metal-semiconductor work function difference is to produce an additional shift of the C-V curve along the voltage axis. In the view of the above discussion a practical MOS structure can be represented by the Figure[5] .

3.6 Flat Band Voltage

In a practical MOS structure all the above mentioned effects may be present simultaneously so that they have to be combined together. A quantity V_{FB} called the flat band voltage defined as the voltage required at the gate of

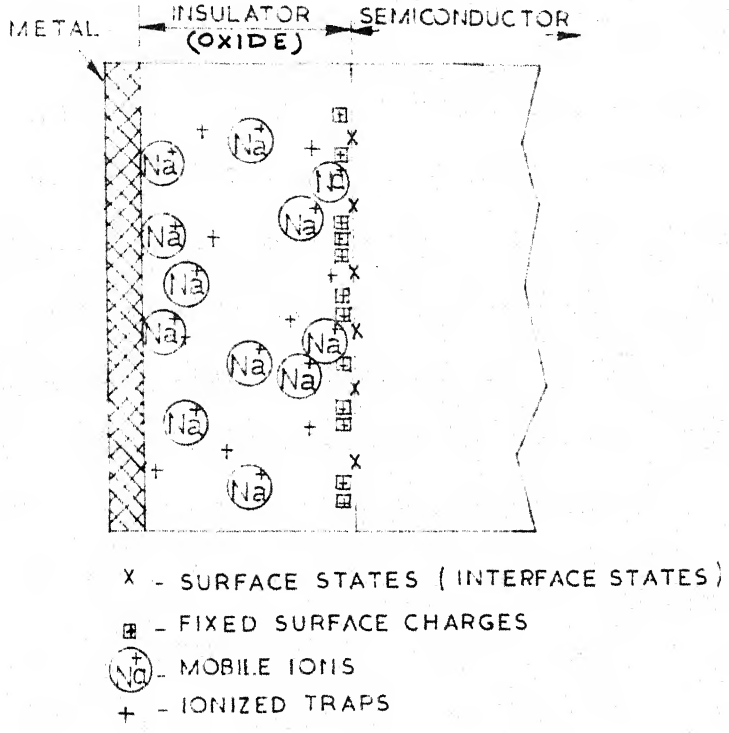


FIG. 5 SHOWING SURFACE STATES AND OXIDE CHARGES IN A PRACTICAL MOS STRUCTURE

the MOS structure to bring about the flat band conditions at the surface, is used to incprocrate all th se effects. Thus

$$V_{FB} = -(\phi_{ms} + (Q_{ss}/C_{ox}) + (1/C_{ox}) \int_0^{d_{ox}} \frac{x}{d_{ox}} \rho(x)\, dx$$

where first term within the parenthesis appears due to metal-semiconductor work function difference, the second term accounts for the surface state charge and the third term takes into account the effects of the oxide charge. Here d_{ox} is the oxide thickness and $\rho(x)$ is the charge density in the oxide layer. V_{FB} can be obtained from the shift of the practical C-V curve with respect to ideal C-V curve along the voltage axis.

Chapter IV

EXPERIMENTAL WORK

FABRICATION TECHNIQUES FOR MOS STRUCTURE

MOS (Metal-Oxide-Semiconductor) structure is one of the fundamental tools to study the surface and other properties of oxidized silicon. An MOS structure was used in the present work to measure the dielectric strength and dielectric constant of silicon dioxide and also the density of surface states at the silicon-silicon dioxide interface. In this chapter a detailed account of the experimental work is given.

4.1 Material Specifications

Chemically polished N-type silicon wafers (P-type high resistivity wafers were not available) supplied by General Diode Corporation, Framingham, Massachusetts 01701. were used for the fabrication of MOS structures. For the determination of surface state density, 11 ohms cm wafer was employed. Particularly for this measurement high resistivity wafer was chosen because of the reasons mentioned in Section 3.4 of Chapter III. For other experiments 0.5 ohm-cm silicon wafers were employed.

A polished silicon surface is a prerequisite for good oxide growth. Without the smooth, clean surface, the structure of the grown oxide tends toward cristobalite

which is undesirable in all the common uses of oxide films in integrated silicon device technology. Cristobalite is denser than silica glass and the boundaries between the amorphous regions and the denser crystalline regions are porous to both surface contamination and impurities during diffusions. Isolated regions of oxide mask failure during diffusion can sometimes be traced to the presence of localized regions of cristobalite in otherwise amorphous oxide.

Prior to oxidation, the wafer surface was examined under microscope and if any damage was detected the wafer was treated with the silicon polishing solution. The solution used in this work consisted of[26]

600 ml nitric acid
200 ml acetic acid
100 ml hydrofluoric acid
10 ml hydrofluorosilicic acid

In view of economy instead of full wafers, the experiments were made on small chips of silicon. These small chips were cut with the help of Kulicke and Soffa wafer scriber supplied by Kulcke and Soffa manufacturing Co., Fort Washington, P.A.

4.2 Importance of Cleanliness in Electron Device Fabrication

Needs for growing high quality oxide have been already stressed at more than one places in this report.

In a recently developed class of silicon devices, in which silicon dioxide film is an active and integral part of the device, the device characteristics very critically depend on its properties. Also, there is another class of silicon devices such as surface tetrode which depend on minority carriers for their operations. The performance of these devices is even more sensitive to the quality of the oxide film. For such applications only very superior quality oxides are employed.

Superior quality oxides can only be grown if adequate attention is paid to the overall cleanliness during their formation. A sizable portion of this chapter has been devoted to the various cleaning operations necessary for growing good oxides.

4.3 Cleaning Procedures

Before the cleaning procedures are described, there is a word of warning "The cleanliness, before, during and after oxidation is the most import requirement for growing high quality oxides. Contamination from any source and at any stage of cleaning can invalidate the entire cleaning operation. Hence the complete cleaning operation must be done with utmost care and sincerity".

This being the first work of this kind carried out in the Integrated Circuits Lab. in I.I.T. Kanpur, it has been felt necessary that the cleaning procedures should be described in greater detail than needed in a well

established laboratory where oxidation is a routine process. This will enable the future workers interested in this field to benefit from the experience gained during this work.

The various measures of cleanliness adopted in the present work are described below:

The purity of the chemicals used in cleaning, is a very important factor. Whenever a new bottle of a chemical is opened, it should be throughly cleaned in running tape water and dried up before opening to avoid any contamination of the chemical. In the present work mostly the BDH Chemicals were used which yielded fairly good results.

Cleaning Procedure for Quartz work Tube

The purity of the materials used in the oxidation process and that of the apparatus in which the oxidation is performed clearly influence the impurity content of the oxide film. Silica glass more popularly known as "Quartz" is regarded as the most acceptable material for building thermal oxidation appratus. The work tube must be very clean in order to avoid any contamination when the oxidation is in progress. For cleaning the quartz work tube, the following practice was adopted.

(a) Fill the tube completely with 5% HF and leave it overnight.

(b) Remove HF, wash the tube througly in running tape water.

(c) Soak in 1% Hot KOH (95°C) for 5 minutes.

(d) Rinse in running tape water.

(e) Soak in Cromic acid for 5 minutes.

(f) Wash in tap water

(g) Finally rinse in D.I. water and dry in the hot furnace.

The same method was used for cleaning quartz thermocouple tube, pull rod and quartz boat. The work tube was kept always closed by a cork to avoid contamination. Similarly, the pull rod and the thermocouple tube were always kept in glass tube casing to protect them from being contaminated. The wafer carrier or boat was always stored in the work tube.

Cleaning Procedures for the Utensils Used in Silicon-Wafer Cleaning Operations

For cleaning the silicon wafers before oxidation, the beakers, measuring cylinders and funnels used, should be thoroughly cleaned. The cleaning procedure is as follows:

(a) Scrub in Vim or Surf or similar detergent.

(b) Rinse thoroughly in running tap water to remove the detergent.

(c) Dip for 10 minutes in 1% (V/V) sodium hydroxide solution at 95°C. This dissolves fatty materials by saponification action.

(d) Rinse thoroughly in running tap water to remove NaoH and the dessolved fatty materials.

(e) Dip in Cromic acid for 5 minutes. The cleaning effect of cromic acid is due to the conversion of some oxides and greases into water soluble compound.

(f) Wash in running tap water.

(g) Finally rinse in DI water and keep inverted for drying in a clean dry tray.

Note:

The cromic acid used in glass were cleaning is prepared by making a saturated solution of Potasium dicromate ($K_2Cr_2O_7$) in the concentrated sulphuric acid. This acid is stored in a big breaker or bottle and is repeatedly used for cleaning.

Cleaning Procedure for Silicon Wafers[26,27]

Sources and Nature of Contaminants:

Since the impurities present on the silicon surface prior to oxidation or during the oxide growth itself influence the homogeneity of the film and the interface electrical properties it is very much necessary that the wafer surfaces must be absolutely free from any surface contamination before they are introduced into the oxidation furnace. It is desirable to analyse comprehensively the various types, sources and effects of surface contaminants before an attempt is made to describe the cleaning procedures.

Surface contaminants can be classified broadly as

(a) Molecular

(b) Ionic

(c) Atomic.

(a) Molecular Contaminants:

Typical molecular contaminants are natural and synthetic waxes, resins and oils. These are typically present after the mechanical grinding, lapping and polishing operations of wafers. They may also include grease from fingers and greasy films that are deposited when surfaces are exposed to room air. Photoresists and organic solvant residues also fall into this category. Layers of such molecular impurities in contact with the substrate surface are usually held by weak electrostatic forces. Organic contaminants on silicon devices, specially on surface sensitive MOS structures, may cause polarization and ionic drift due to the transport of protons. Water-insoluble organic compounds tend to make semiconductor and oxide surfaces hydro-phobic, thus preventing the effective removal of adsorbed ionic or metallic impurities. The elimination of molecular contaminants should therefore be considered the first step in a cleaning process.

(b) Ionic Contaminants:

They are present after etching of wafers in HF containing etchents or in caustic solutions even after extensive rinsing in DI water. They may deposite on the

silicon surface by physical adsorption or by chemisorption. The removal of chemisorbed ions is much more difficult than the removal of ions attached to the surface by physical forces, and a chemical reaction must generally be used to achieve desorption. Of the ionic contaminants alkali ions are particularly harmful in that they may move under the influence of electric fields or at elevated temperatures, causing inversion layers, surface leakage, drifts during device operation.

(c) Atomic Contaminants:

These include heavy metals such as gold, silver and copper. They originate from acid silicon etchants and are usually plated out in the form of metallic deposites. The removal of this type of contaminant generally requires reactive agents that dessolve the metal and complex the ionic form to prevent redeposition from the solution. Atomic impurities, especially the heavy metals, can seriously affect minority carrier life time, surface conduction and other device parameters governing stability of devices.

Since a contaminated surface is likely to contain all three types of impurities, it is necessary to first remove the gross organic residues masking the surface, then the resudual organic materials and finally the residual ionic and atomic contaminants.

Different laboratories report different procedures for wafer cleaning, the method used in this work is described below. As mentioned earlier the order of the steps used in cleaning operation is important and should be strictly followed.

Procedure for Silicon Wafer Cleaning[26,27,28]

Cleaning operation	Approx. time recommended	Types of Impurities removed
(a) Heat in Trichloethylene	10 minutes	Molecular impurities, such as Waxes, Resins and oils.
(b) Ultrasonic agitation in methanol	5 minutes	Enhances dessolution of of residues by local stirring action.
(c) Heat at 95°C in a solution of equal parts of H_2O_2(6%), NH_4OH and DI water	30 minutes	Organic contaminants that are attacked by both the solvating action of NH_4OH and the powerful oxidizing action of the hydrogen peroxide. The NH_4OH also serves to complex some group I and II metals, such as, Cu, Ag, Ni, Co and Cd.
(d) Rinse in DI water and agitate ultrasonically.	5 minutes	To remove the reagents used in (c).

Cleaning operation	Approx. time recommended	Types of impurities removed
(e) Heat in conc. HNO_3.	10 minutes	To remove heavy metals.
(f) Ultrasonic agitation in HNO_3.	5 minutes	-
(g) Rinse several times in hot DI water	-----	To remove HNO_3
(h) Immerse in HF	30 seconds	To remove SiO_2 from the surface of the wafer.
(i) Rinse and agitate in ultrasonic cleaner in DI water.	5 minutes	To remove HF.

Note:

In order to avoid the formation of excessive pin holes in the grown oxide film, ultrasonic agitation is a must. In ultrasonic cleaning dissolution of residues is enhanced by the intense local stirring action of the shock waves created in the solvent. Thus, solvent saturated with impurities is continually carried away from the wafer surface and fresh less saturated liquid is admitted. Mechanical vibrations induced in the wafer further aid in loosening gross contaminants.

After the cleaning operation was over, the wafer was removed from the DI water with the help of a tweezer and immediately placed dripping wet on a hot quartz boat. After about 5 minutes the boat was carefully pushed to a preselected spot on the temperature profile. A mark was made on the push rod to facilitate the placement of the boat at the proper depth. Oxygen gas was then made to flow at a desired rate which was maintained constant till the end of the oxidation. The time required for a given oxide thickness under a particular set of oxidation conditions, was estimated from standard plots. Description of the oxidation set-up used in the present work has been given in Chapter 2 of this report.

4.4 Oxide Etching from Non-polished Surface

In order to make ohmic contacts to the un-polished silicon surface the oxide from that surface must be removed. For removing the oxide, a thick layer of Apizone wax dissolved in trichloroethylene was applied on the polished surface with the help of a fine brush. The wax coating must be sufficiently thick and sufficient time must be allowed (about one hour) to get the wax coating completely dried up. If this is not done, some pin holes may be left in the wax coating and the oxide layer on the polished surface will be dissolved by HF through these holes. This will render the preserved oxide useless for further experimentation. This difficulty was experienced at the

earlier stages of the present work, however, as more experience was gained it was overcome by taking the precautions described above.

The oxide on the nonpolished side was etched by dipping the wafer in 48% HF for 30 seconds. The wax was removed by boiling the wafer in trichlorothylene 3 to 4 times till the traces of wax were completely removed from the oxide surface. A simple method to test the complete removal of oxide is by water flow method in which water does not stick to Si surface but stickes to SiO_2 surface.

4.5 Al-Metallization

The MOS structure was completed by providing Al metal contacts. Al was chosen because it is very easy to evaporate and it provides good ohmic contact with Si and SiO_2. Al. films have very good adherence both on Si and SiO_2 surfaces.

There are two common methods of thin film deposition:

(a) Film deposition through metal masks

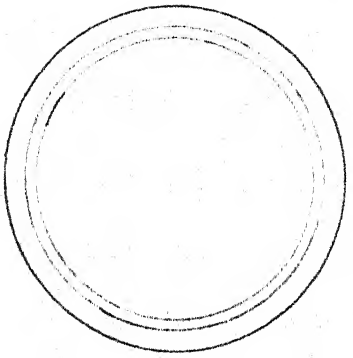
(b) Photolithographic Techniques.

As the clean room was not ready, photolithographic method was not tried. Al. was deposited by vacuum evaporation through metal masks.

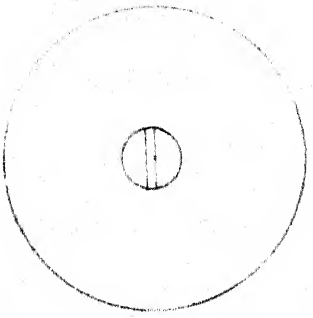
Film Deposition Through Metal Masks[28]

According to the need and suitability the different diameters Al. dots were deposited. In some experiments the Al. dots dia. was as small as 250 microns in order to cover the smallest no. of pin holes present in the oxide film, if any. In other experiments the Al-dots dia. was kept as large as 500 microns in order to obtain a reasonably large value of MOS capacitance. In barrier height measurement, the Al-dot dia was still larger in order to have sufficient space for lead connection. The masks suitable for different experiments were fabricated in the Precision Workshop from a 5 micron thick copper sheet. A special type of mask holder shown in the Figure 6 was also fabricated in the Precision Workshop. The mask holder consists of threaded outer and inner parts. The wafer along with the mask was enclosed in the mask holder assembly which ensures a very good physical contact between the two.

In order to have good circular Al. dots deposited on the wafer two things are important. First, the mean free path of the evaporant particles must be long compared with the mask-to-wafer spacing to avoid random condensation caused by intermolecular collisions. Second, the sticking coefficient of the impinging vapor must be close to unity to prevent re-evaporation and lateral spreading under the mask. When evaporating in a high vacuum and with the mask in physical contact with the wafer these prerequisites are

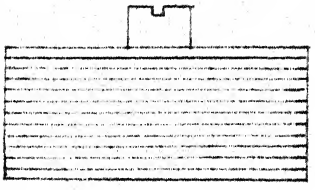


Plan

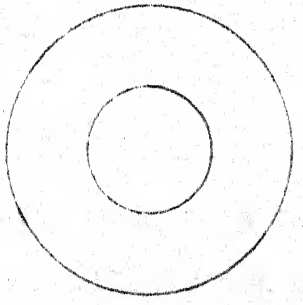


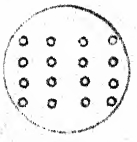
Plan

Elevation



Elevation





Cu mask
5 μ thick

FIG·6 COMPONENTS OF A MASK HOLDER ASSEMBLY

usually satisfied. In the present work the vacuum used was in the range of 10^{-6} torr which satisfies the first condition. The second condition was met by enclosing the wafer and mask in a special mask holder described above.

Al. film was deposited on the other side of the wafer so that the contribution of the capacitance on this side to the total capacitance can be neglected.

In order to deposte a homogeneous and uniform Al. film which is free from pin holes and has good adherence to the sample surface, it is necessary to stress upon the cleanliness of the sample surface, the mask and that of the mask holder. The various methods used for cleaning are briefed below:

Sample surface cleaning

After the oxide from non-polished surface was etched the sample was cleaned as follows:

(a) Heat in TCE for 5 minutes.

(b) Heat in Acetone for 5 minutes.

(c) Ultrasonic agitation in methanol for 2 minutes.

(d) Store in methanol till loaded in vacuum system.

Mask and Mask Holder Cleaning

If the mask has not been previously used, it should be very thoroughly cleaned and inspected prior to use. Dust particles, fibres or debris from the machining process may cause discontinuities in the deposited film. For cleaning

masks and mask holder ultrasonic agitation in organic solvents was employed in this work. The procedure is given below.

(a) Boil for 10 minutes in aqueous detergent solution. Surf was used for the present work.

(b) Wash in running tap water.

(c) Heat in TCE for 5 minutes

(d) Ultrasonic agitation in Acetone for 5 minutes.

(e) Ultrasonic agitation in methanol for 5 minutes.

Al- used for contact deposition was 99.9995% pure. Before use it was cleaned by ultrasonic agitation in organic solvents and finally heated in dil. Hcl acid for 10 minutes. Then it was rinsed in DI water and stored in methanol till used.

Resistance heating was employed, the source (Al) was heated from a tungston spiral. The tungston spiral was also cleaned by ultrasonic agitation in common cleaning solvents such as TCE, acetone and methanol respectively. Further cleaning of the tungston spiral was done by degasing the filament in high vacuum (10^{-6} torr range) by allowing little more current than actually used during evaporation, so that all contaminants come out from the surface of the spiral.

Note: The processed wafers were stored in a very clean dry container having threaded lid. The container carrying these wafers was tightly closed and stored in a decicator containing fused calcium chloride.

Chapter V

MEASUREMENTS AND RESULTS

During the course of this work two types of measurements were made,

(1) Optical measurements for the determination of oxide thickness.

(2) Electrical measurements on MOS structure for the evaluation of electrical properties of thermally grown oxide films.

In this chapter a brief description of these measurements will be presented.

5.1 Oxide Thickness Measurement

Precise control of oxide thickness is of paramount importance in silicon device fabrication especially in the fabrication of integrated circuits. From the beginning of this work, considerable amount of time was spent in obtaining reproducible oxide films. Oxide thickness measurements were made on a Unitron Series N Metallograph supplied by Unitron Instrument Co. This instrument is converted into a multiple-beam micro-interferometer by using interference accessories supplied with the metallograph. The measurement of oxide thickness by this method requires the formation of a step on the oxide layer. The following procedure was used for forming wedge-shaped step in the grown oxide films on silicon.

A thick layer of apiezon wax dissolved in toluene or trichloroethylene was applied with a brush to a portion of the silicon specimen surface possessing the oxide film. This was allowed to dry up at least for one hour till the wax was completely dried. A uniform thick wax coating was found necessary to avoid any possibility of the liquid etchant reaching the protected side of the oxide and etching a hole in it. The specimen was then immersed for nearly 60 seconds in 48% HF to dessolve the unprotected portion of the oxide film. After this the specimen was thoroughly rinsed in DI water and the wax was removed with trichloroethylene.

The surface of the specimen including the step was then metallised by evaporating a thin film of high purity Al. on it in a high vacuum system. The evaporation was performed at pressure of about 10^{-6} torr. This was found necessary in order to obtain bright and well defined fringe pattern. Al. metallization process has already been described in section 4.5 of this report.

The thickness of the oxide film was calculated from the fringe patter by the relation,

$$d_{ox} = \left(\frac{D}{B}\right) \left(\frac{\lambda}{2}\right) \text{ microns}$$

where λ = 644 m u for cadmium monochromatic light used in the thickness measurement, and

D and B are defined in the Fig. 7 .

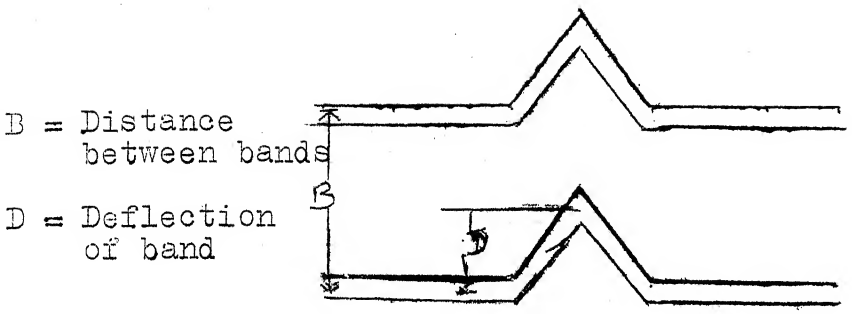


Fig.7

Other methods which are sometimes employed for oxide thickness measurements are

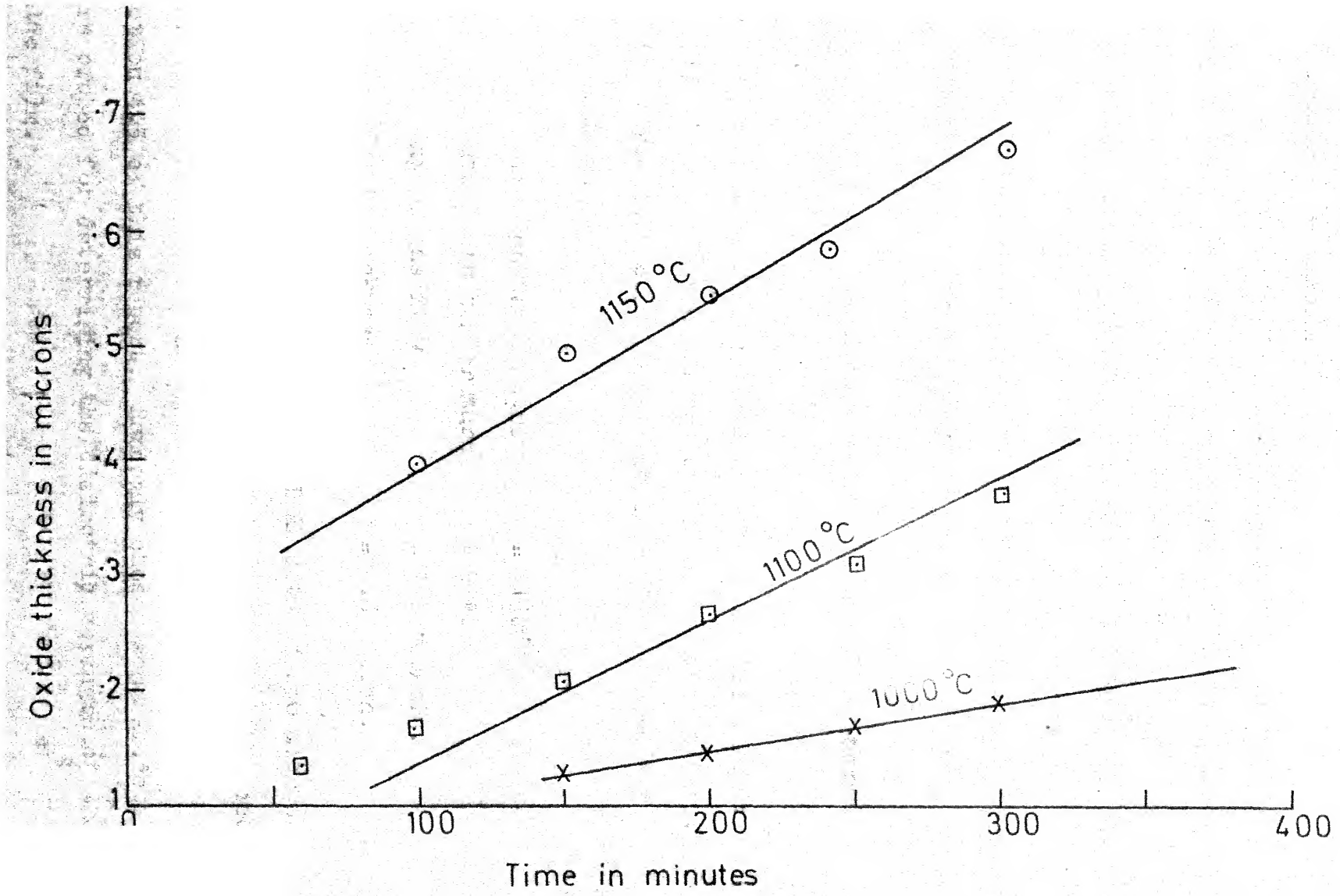
(i) Weighing of sample, and

(ii) Thickness estimation from its colour.

The first method involves the weighing of the sample before and after oxidation in a micro-balance. This method requires the knowledge of film area and its density in order to convert weight into thickness.

The second method so-called the colour method consists of comparing the colour of unknown film with the colours of a set of standard films of different thicknesses. This method is applied between the thickness 500-4000Å with an accuracy of ±200Å.

The particular colour of a film arises from the interference between the light beams from the upper and lower surfaces of the oxide film. Reflection of specific wave lengths interfere destructively and the remaining wave lengths combine to give a characteristic colour to the oxide film depending upon its thickness.



OXIDE GROWTH RATE IN DRY OXYGEN

FIG. 7a

5.2 Electrical Measurements

All the electrical measurements during this work were made on an MOS structure employing the Electroglass wafer prober model 131 shown in the Figure 8. A tungston probe making contact with the metal dot (gate) provided one lead and the other lead was directly taken from the metallic vacuum chuck which was in intimate contact with the metallised silicon surface. To ensure good contact between the silicon and vacuum chuck, all the uncovered holes of the vacuum chuck were closed with a thick gummed paper.

(a) Measurement of Dielectric Strength of the Oxide Film:

(i) Sample: N-type silicon of 0.5 ohm-cm resistivity.

(ii) Oxidation conditions: Wet oxidation process was used.

Oxidation temperature	= 1150°C
Water bath temperature	= 90°C
Oxygen gas flow	= 1 liter/min.
Oxide thickness	= 0.6 micron.

For this experiment, several Al.dots of 250 microns dia. each were evaporated on the oxide surface by the vacuum evaporation of Al. through Cu. mask as described in Section 4.5 of this report. Randomly chosen some Al.dots were probed for determining the dielectric strength of the oxide film.

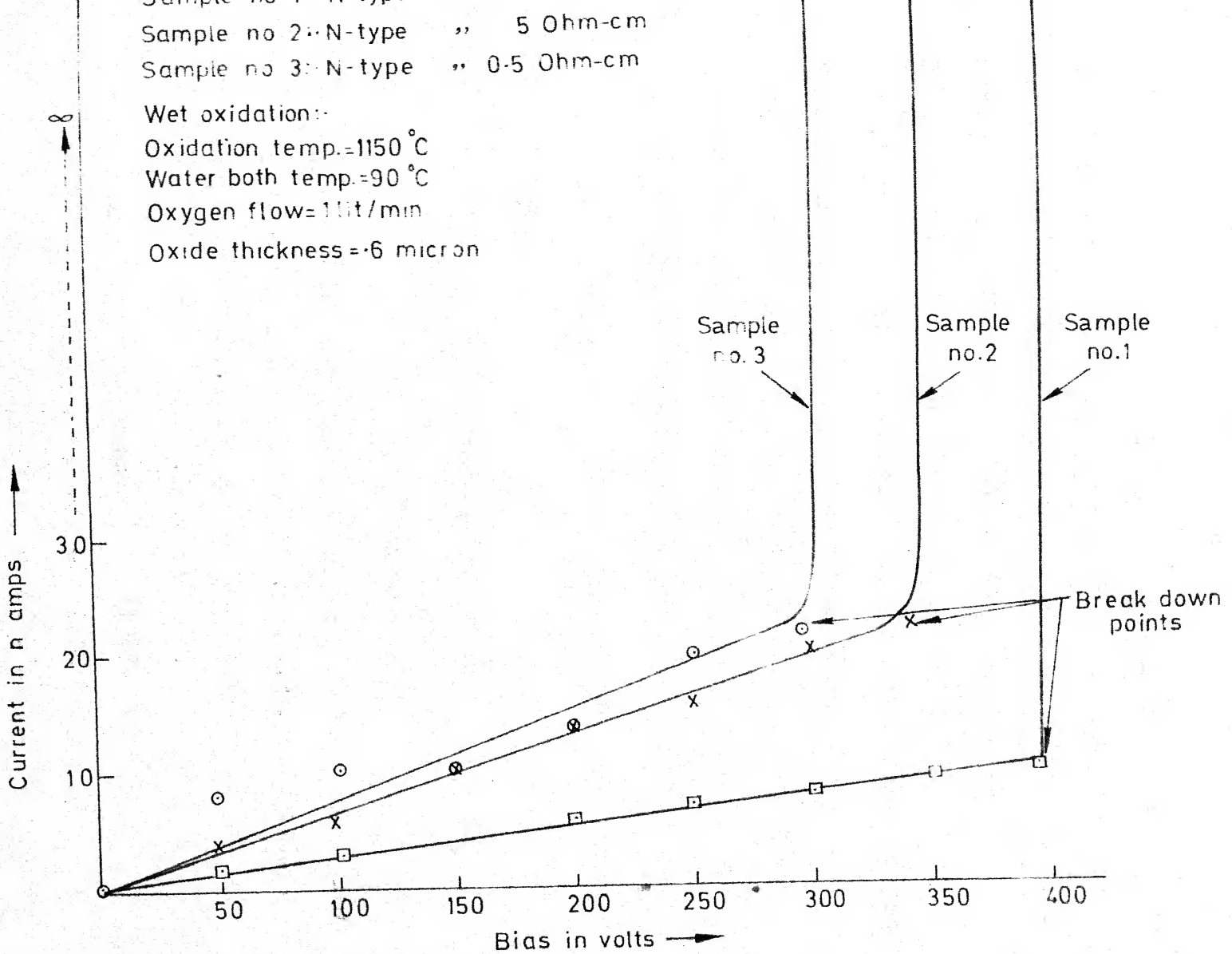


Fig-8 Showing break down of oxide films

For measuring small currents a sensitive D.C.meter (model 95A, Boonton Electronic Corporation, USA) was used and the D.C. voltage was applied from a D.C. Power Supply. Some of the recorded observations are plotted in Figure 9. It is obvious from these curves that at pre-breakdown voltages the currents for various samples do not differ much from each other and the breakdown of the oxide film is very sharp and well defined. These facts indicate that the quality of the grown oxide is sufficiently good for its various applications mentioned in Chapter I.

Considering the minimum value for breakdown strength, from Figure

$$E_{breakdown} = \frac{300 \times 10^4}{0.6} \text{ volts/cm}$$

$$= 5 \times 10^6 \text{ volts/cm.}$$

(b) Measurement of Dielectric Constant of the Oxide Film:

Sample: N-type silicon of 0.5 ohm.cm. resistivity.

Oxidation conditions: Dry - Wet. - dry combination was used.

Oxidation temperature = 1100°C

Water bath temperature = 90°C

Oxygen gas flow = 1 liter/min.

Oxide thickness = 0.5 micron.

In general, the most convenient and accurate method of making measurements on an MOS structure is to mount it on a TO-5 header in such a way that its semiconductor side is in contact with the body of the header. Necessary terminals are then obtained by means of a TC or ultrasonic bonder.

As the bonding facilities were not available during the course of this work, the MOS structure, therefore, was probed on the same wafer prober that was used in the measurement of the dielectric strength.

The connection between the the wafer prober and the test posts of the capacitance bridge was made using co-axial cable of minimum possible length in order to minimise the leads and the stray capacitances. "Remote" test posts were used and the instructions of the "operation manual" were strictly followed for maximum accuracy.

Capacitance of the MOS structure was measured under heavy "accumulation" in order to obtain the true capacitance of the oxide film. Out of 12 Al.dots (dots. dia 250 microns) only 3 randomly chosen dots were probed Some of the recorded observations are reproduced below:

First Dot:

S.No.	Bias in volts	Capacitance in PF
1	0	3.30
2	5	3.30
3	10	3.30
4	15	3.30
5	20	3.30
6	25	3.35
7	28	3.36

Second Dot:

Sl.No.	Bias in volts	Capacitance in PF
1	0	4.2
2	5	4.2
3	10	4.12
4	15	4.2
5	20	4.14
6	25	4.18
7	28	4.18

Third Dot:

1	0	3.41
2	5	3.41
3	10	3.42
4	15	3.42
5	20	3.43
6	25	3.46
7	28	3.47

The difference in the values of the measured capacitance may be probably due to local fluctuations in the carrier concentration of the silicon wafer and also due to difference in the areas of the various Al. dots.

Calculations:

The average value of the capacitance from the above observations is given by

$$C_{average} = \frac{3.30 + 4.2 + 3.37}{3} = 3.66 \text{ PF}$$

Area of Al.dot $= \frac{\pi D^2}{4} = \frac{3.14}{4} \times (\frac{1}{40})^2$ cm^2

$= 4.9 \times 10^{-4}$ cm^2

Hence the capacitance per cm^2 of the oxide layer

$$= \frac{3.66 \times 10^{-12}}{4.9 \times 10^{-4}} = 7.4 \times 10^{-9} \text{ F}.$$

$= 7.4$ nF.

Thus, the average dielectric constant of the oxide film

$$\epsilon_{ox} = \frac{2.4 \times 10^{-9} \times 5 \times 10^{-5}}{8.85 \times 10^{-14}} = 4.2 \text{ at 100 KHz}$$

(c) Determination of Surface State Density at $Si-SiO_2$ Interface:

(i) High frequency measurement (100 KHz)

Sample: N-type 11 ohm-cm resistivity.

Oxidation conditions: Dry oxidation was employed.

Oxidation temperature	= 1100°C
Oxygen gas flow	= 1 liter/min.
Oxygen pressure	= 1 atm.
Oxide thickness	= 0.2 micron.

Here, techniques of measurement as well as the precautions to be taken, are the same as described in the case of dielectric constant measurement.

Some of the recorded observations are given below:

Positive Bias (Accumulation):

Sl.No.	Bias in volts	Capacitance in PF	Normalised value $C_n = \frac{C}{C_{ox}}$
1	0	22.27	0.97
2	5	22.27	0.97
3	10	23.02	1.00
4	15	23.03	1.00
5	20	23.04	1.00
6	25	23.04	1.00
7	28	23.04	1.00

Negative Bias (Depletion):

1	0	22.26	0.97
2	1	22.16	0.965
3	2	21.94	0.945
4	3	21.04	0.915
5	4	19.76	0.86
6	5	17.04	0.775
7	6	14.96	0.650
8	7	12.30	0.535
9	8	10.00	0.436
10	9	8.41	0.366
11	10	7.75	0.338
12	11	7.45	0.327
13	12	7.50	0.326
14	13	7.50	0.326
15	14	7.60	0.330
16	15	7.70	0.330

Calculations of Theoretical Curve:

In Chapter III of this report, detailed theory of $Si-SiO_2$ interface has been given. Some of the formulae needed for calculations of theoretical curve are reproduced here for quick reference.

(i) $$V_{app} = \frac{Q_{sc}}{C_{ox}} + \phi_s \qquad (3.6)$$

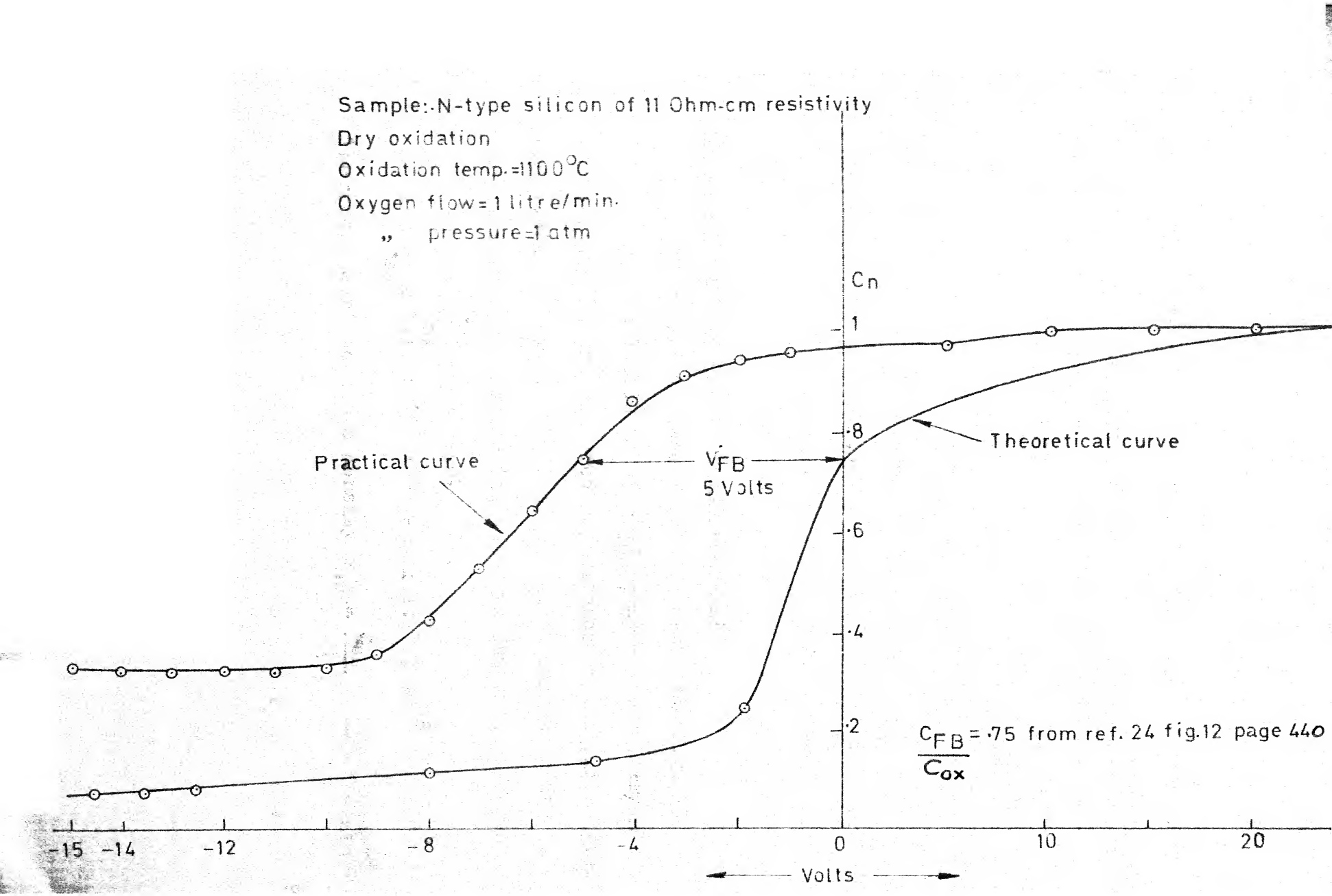
(ii) $$Q_{sc} = -2\left(\frac{u_s}{|u_s|}\right) q\, n_i\, L_D \left\{2\left[\cosh(u_s - u_B) - \cosh u_B + u_s \sinh u_B\right]\right\}^{\frac{1}{2}} \qquad (3.4)$$

with some trigonometrical modification.

(iii) $$\frac{C}{C_{ox}} = \frac{1}{1 + \sqrt{\frac{2\epsilon_{ox}^2}{q\, N_A\, \epsilon_s\, d_{ox}^2}\, V_{app.}}} \qquad (3.18)$$

The first step in calculation is to determine the values of Q_{sc} from equation (3.4) corresponding to various values of u_s given by $u_s = \frac{q\,\phi_s}{kT}$, where $\phi_s = \frac{Y}{\beta}$, Y being the surface potential relative to bulk and is equal to the band bending in "kT" units. $\beta = \frac{q}{kT} = 38.5$ at room temperature.

Once Q_{sc} is known, corresponding values of $V_{app.}$ are calculated from equation (3.6) and value of $C_n = C/C_{ox}$ are then determined by substituting the values of $V_{app.}$ in equation (3.18).


Sample:-N-type silicon of 11 Ohm-cm resistivity
Dry oxidation
Oxidation temp.=1100°C
Oxygen flow=1 litre/min.
„ pressure=1 atm
Cn
1
·8
·6
·4
·2
Practical curve
Theoretical curve
V_{FB}
5 Volts
$\frac{C_{FB}}{C_{ox}}$ = ·75 from ref. 24 fig.12 page 440
-15
-14
-12
-8
-4
0
10
20
Volts

The results have been recorded in the following table.

S.No.	V_{app} in volts	$C_n = \frac{C}{C_{ox}}$
1	-0.0	0.75
2	-1.90	0.252
3	-4.712	0.193
4	-8.064	0.110
5	-12.5	0.09
6	-13.77	0.087
7	-14.674	0.0835

Calculation of Surface States Density:

Flat band voltage V_{FB}=5.00 volts from fig. 10

C_{ox} in Farads/cm^2 = $\frac{23.04}{1.96\times10^{-3}}$ = 1.17×10^{4} PF/cm^2

where 23.04 is the measured capacitance of the oxide layer and 1.96×10^{-3} cm^2 is the area of Al.dot corresponding to 500 microns dia. Neglecting the work function difference

$$V = \frac{Q_{ss}}{C_{ox}} = 5.0V$$

$$Q_{ss} = 1.17 \times 10^4 \times 5 = 5 \times 1.17 \times 10^{-8} \text{ coub/cm}^2$$

Therefore Surface state density $N_{ss} = \frac{Q_{ss}}{q} = \frac{5\times1.17\times10^{-8}}{1.6\times10^{-19}}$

$$= 3.66 \times 10^{11} \text{ Stats/cm}^2$$

The work function difference was found by calculation to be 0.1 V which can be neglected. Hence No. of surface states is 3.66×10^{-11} states per cm^2 at 1000 KHz

Low Frequency Measurements

These measurements were made on a impedance bridge obtained from General Radio Company Concord, Mass. U.S.A. Boonton Capacitance bridge could not be used because it does not have any provision for applying low frequency signal. Some of the results are shown in Table below.

(a) Measuring Frequency 100 Hz: (Positive Bias)

Sl.No.	Bias in volts	Capacitance in PF
1	0	23.6
2	5	23.6
3	10	23.6
4	15	23.6
5	20	23.6
6	25	23.6
7	30	23.6

Negative bias:

Sl.No.	Bias in volts	Capacitance in PF
1	0	23.6
2	3	23.3
3	6	22.2
4	9	12.8
5	12	13.7
6	15	18.91
7	13	21.7
8	21	22.3
9	24	22.3
10	27	22.3
11	28	22.3

(b) Measuring frequency 50 Hz: (Positive Bias)

1	0	23.6
2	5	23.6
3	10	23.6
4	15	23.6
5	20	23.7
6	25	23.7
7	28	23.7

(Negative bias):

1	0	23.6
2	3	23.3
3	6	20.4
4	9	12.8
5	12	13.7

Positive Bias (continued):

6	15	18.7
7	18	21.1
8	21	21.7
9	24	21.9
10	27	21.9
11	28	21.9

5.3 Concluding Remarks:

In the table shown below, a comparison has been made between the values obtained during the present work and obtained by similar investigations by other workers.

S.No.	Quantity	Value obtained in the present work	Value cited in the literature	Ref.
1	Dielectric strength	5×10^{6} volts/cm	10^{6}-10^{7} V/sec.	26
2	Dielectric constant	4.20	3.78 to 10	26
3	Density of surface states	$4.6\times10^{11}/cm^{2}$	10^{11} to 10^{12}/ cm^{2}	18

The above results indicate that the quality of the grown oxides is sufficiently good and can be employed for the fabrication of planar transistor as well as for many other components used in integrated circuits. Also as can be seen from Figure , the obtained results are in good qualitative as well as quantitative agreement with theory.

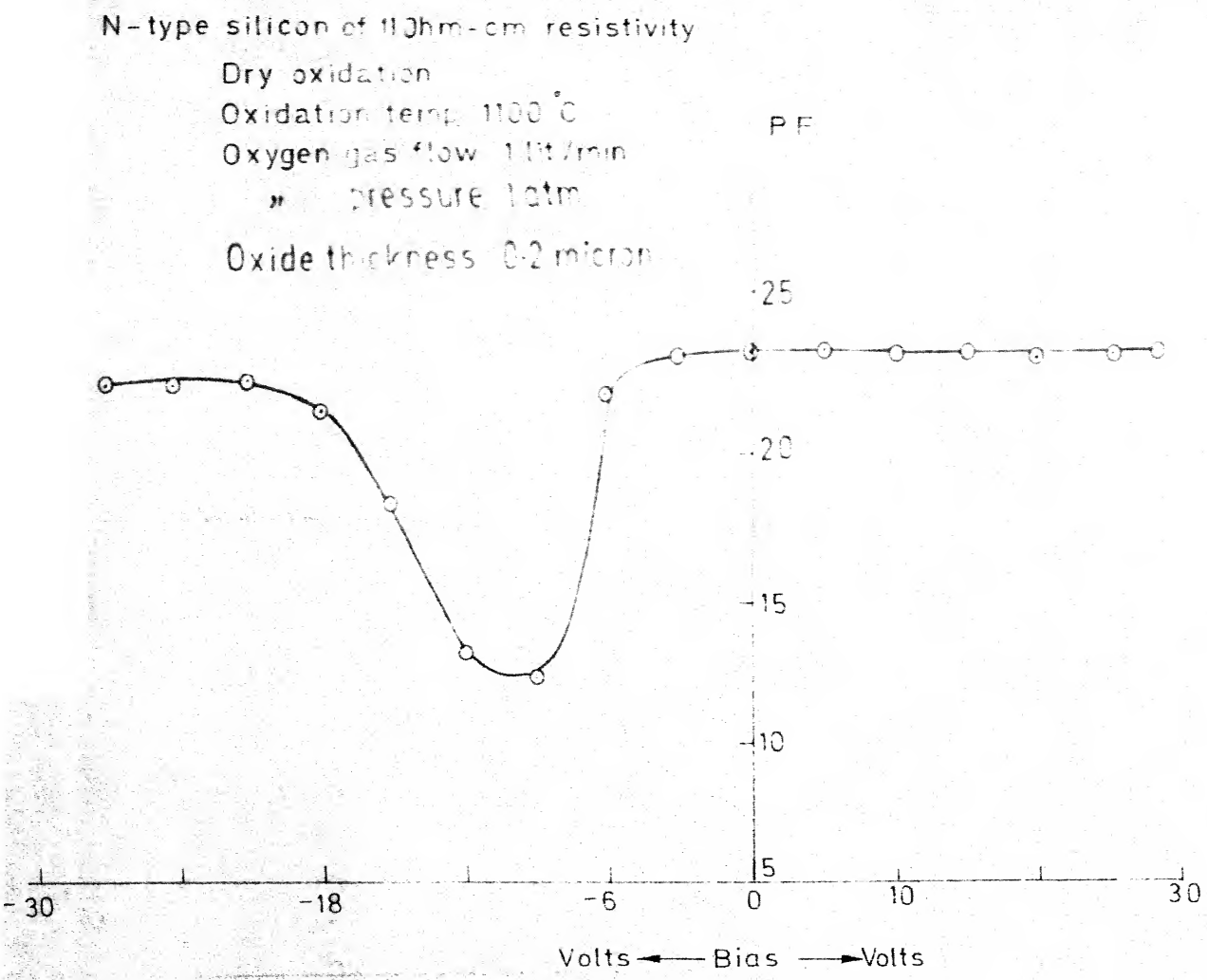


Fig. 11 Showing low frequency (100 Hz) response of a MOS structure

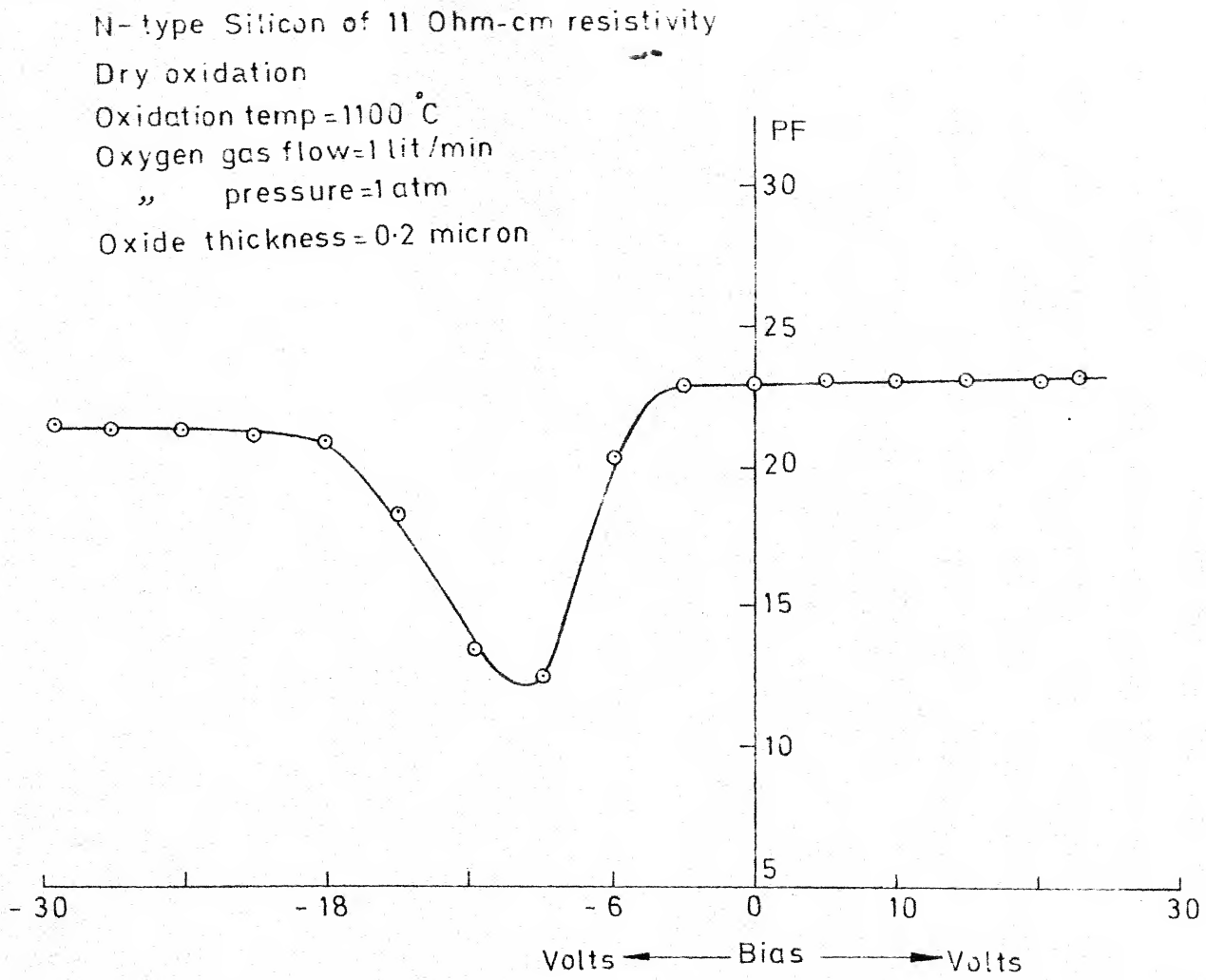


Fig.12 Low frequency (50 Hz) response of an MOS structure

It must be remembered that this work was carried out in a place where clean room facilities were not available. Under these circumstances, it is expected that several types of contaminants might have affected the results obtained in the present investigations. It might be possible that if this work were completed in a clean room, the results would have been much closer to those reported by other workers.

REFERENCES

1. C.T. Sah, H. Sello, and D.A. Tremere, "Diffusion of Phosphorus in Silicon Oxide Film," J. Phys. Chem. Solids 11, 1959, pp. 288-298.

2. A.G. Nassibian and G. Whiting, "SiO_2 Masking Against Phosphorus Diffusion Using a P_2O_5 source," Solid State Electron 7, Dec. 1964, pp. 873-878.

3. S. Horiuchin and Yamaguchi, "Diffusion of Boron in Silicon Through Oxide Layer," Japan J. Appl. Phys. 1, 1962, p.374.

4. L.V. Gregor, "Passivation of Semiconductor Surfaces," Solid State Tech. 14, April 1971, pp. 37-43.

5. J.R. Ligenza, "Oxidation of Silicon by High-Pressure Steam," J. Electrochem. Soc. 109, Feb. 1962, pp. 73-76.

6. B.E. Deal, " The Oxidation of Silicon in Dry Oxygen, Wet Oxygen and Steam," J. Electrochem. Soc. 110, June 1963, pp. 527-533.

7. J.R. Ligenza, "Effect of Crystal Orientation on Oxidation Rates of Silicon in High-Pressure Steam," J. Phys. Chem. 65, Nov. 1961, pp. 2011-2014.

8. P.J. Jorgensen, "Effect of an Electric Field on Silicon Oxidation," J. Chem. Phys. 37, Aug. 1962, pp. 874-877.

9. P.F. Schmidt and W. Michel, "Anodic Formation of Oxide Films on Silicon," J. Electrochem. Soc. 104, April 1957, pp. 230-236.

10. J. Klerer, "A Method for the Deposition of SiO_2 at Low Temperatures," J. Electrochem. Soc. 108, Nov. 1961, pp. 1070-1071.

11. A.S. Grove and D.J. Fitzgerald, "Surface Effects on p-n Junctions-Characteristics of the Surface Space-charge Region Under Non-equilibrium Conditions," Solid State Electron 9, 1966, pp.783-

12. A.S. Grove, O. Leistiko and W.W. Hooper, "Effects of Surface Fields on the Breakdown Voltage of a Planar Si p-n Junction," IEEE Trans. Electron Devices ED-14, March 1967, pp.157.

13. R. Linder, "Semiconductor Surface Varactor," B.S.T.J. 41, May 1962, pp. 803-831.

14. R.H. Kingston, Seegfried, F. Neustadter, "Calculation of Space-Charge, Electric Field and Free Carrier Concentration at the Surface of a Semiconductor," J. Appl. Phys. 26, 1955, pp. 718-720.

15. Goetzberg, "Ideal MOS Curves of Si," B.S.T.J. Sept. 1966, pp. 1097-1122.

16. A.S. Grove, "Physics and Technology of Semiconductor Devices," John Wiley and Sons Inc. New York.

17. E. Kooi, "The Surface Properties of Oxidized Silicon", Phillips Technical Library, Newyork.

18. A.S. Grove, B.E. Deal, E.H. Snow and C.T. Sah, "Characteristics of the Surface State Charge (Q_{ss}) of the Thermally Oxidized Silicon," J. Electrochem. Soc. 114, March 1967, pp.

19. A.S. Grove, B.E. Deal, E.H. Snow and C.T. Sah, "Investigation of Thermally Oxidized Silicon Surfaces Using MOS," Solid State Electronics 8, Feb. 1965, pp. 145-163.

20. F.P. Heiman and G. Marfield,"The Effects of Oxide Traps on the MOS Capacitance," IEEE Trans. Electron Devices-ED-12, April 1965, pp. 167-178.

21. Kooi, "Surface Charge in Oxidised Silicon," Phillips Research Report 21, 1966, pp. 595-615.

22. M.V. Whelan, "On Nature of Surface States in Si-SiO_2 System," Phillips Research Report 22, 1967, pp.289-303.

23. Revesz and Zaininger, "The Si-SiO_2 Solid State Interface System," R.C.A. Review, 29, 1968, pp.22-76.

24. S.M. SZE, "Physics of Semiconductor Devices, "John Wiley and Sons, New York.

25. A.G. Revesz, "The Defect Structure of Grown SiO_2 Films," IEEE Trans. Electron Devices ED-12, 1965 pp. 97-101.

26. Burger and Donovan,"Fundamentals of Silicon Integrated Device Technology, Volume 1, Prentice-Hall, Inc., Englewood Cliffs, New Jersey.

27. Werner Kern and David A. Puotinen, "Cleaning Solutions Based on Hydrogen Peroxide for Use in Silicon Semiconductor Technology," R.C.A. Review, 31, June 1970, pp.187-206.

28. Maissel and Reinhard Glang,"Hand Book of Thin Film Technology, McGraw-Hill Book Company, New York.

29. Many, Goldstein and Grover, "Semiconductor Surfaces," North-Holland Publishing Company, Amsterdam.

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